What Is Claimed Is:

1. A level-shifting circuit, comprising:

a level modulating circuit having an input terminal and an inverse input terminal for respectively receiving a complementary pair of small signals, and a first output terminal for outputting a voltage level in response to the complementary pair of small signals; and

an enable circuit coupled to the first output terminal and making the first output terminal output a predetermined voltage level signal when receiving a disable signal.

2. The level-shifting circuit as claimed in claim 1, wherein the enable circuit is a MOS transistor having a source and a drain coupled between an external level and the first output terminal, and a gate coupled to the disable signal.

3. The level-shifting circuit as claimed in claim 2, wherein the enable circuit is a first PMOS transistor having the source coupled to a power source, and the drain coupled to the first output terminal.

4. The level-shifting circuit as claimed in claim 2, wherein the enable circuit is a first NMOS transistor having the source coupled to a ground level, and the drain coupled to a second output terminal.

5. The level-shifting circuit as claimed in claim 1, wherein the enable circuit further comprises a pair of second NMOS transistors having drains respectively coupled to the input terminal and the inverse input terminal, sources coupled to the

complementary pair of small signals, and gates coupled to the disable signal.

6. The level-shifting circuit as claimed in claim 4, wherein the enable circuit further comprises a pair of third NMOS transistors having drains respectively coupled to the input terminal and the inverse input terminal, sources coupled to the complementary pair of small signals, and gates coupled to the disable signal.

7. The level-shifting circuit as claimed in claim 6, wherein the enable circuit further comprises an inverter coupled between the gates of the first and third NMOS transistors.

8. The level-shifting circuit as claimed in claim 1, wherein the level modulating circuit comprises:

a first PMOS transistor having a first gate coupled to the input terminal, a first source coupled to a power source and a first drain as the second output terminal;

a second PMOS transistor having a second gate coupled to the reverse input terminal, a second source coupled to and a second drain as the first output terminal;

a third NMOS transistor having a third gate coupled to the power source, a third drain coupled to the first drain and a third source as the input terminal; and

a fourth NMOS transistor having a fourth gate coupled to the power source, a fourth drain coupled to the second drain and a fourth source as the inverse input terminal.

9. A level-shifting circuit, comprising:

a level modulating circuit having a first input terminal for receiving a reference signal and a second input terminal for receiving a modulating signal, and an output terminal for outputting a voltage level in response to the level of the modulating signal; and

an enable circuit coupled to the output terminal and making the output terminal output a predetermined voltage level signal when receiving a disable signal.

10. The level-shifting circuit as claimed in claim 9, wherein the enable circuit is a thin film transistor (TFT) having a source and a drain coupled between an external level and the output terminal, and a gate coupled to the disable signal.

11. The level-shifting circuit as claimed in claim 9, wherein the enable circuit is a first P-type thin film transistor having the source coupled to a power source, and the drain coupled to the first output terminal.

12. The level-shifting circuit as claimed in claim 9, wherein the enable circuit is a first N-type thin film transistor having the source coupled to a ground level, and the drain coupled to a second output terminal.

13. The level-shifting circuit as claimed in claim 9, wherein the enable circuit further comprises a pair of second N-type thin film transistors having drains respectively coupled to the first and second input terminals, sources respectively receiving the reference signal and the modulating signal, and gates coupled to the disable signal.

14. The level-shifting circuit as claimed in claim 9, wherein the enable circuit further comprises a pair of third N-type thin film transistors having drains respectively coupled

to the first and second input terminals, sources respectively receiving the reference signal and the modulating signal, and gates coupled to the disable signal.

15. The level-shifting circuit as claimed in claim 9, wherein the enable circuit further comprises an inverter coupled between the gates of the first N-type thin film transistor and the third N-type thin film NMOS transistor.